REMARKS

This responds to the Office Action mailed on September 5, 2006. Claims 15 and 21 are amended. Claims 1-23 are pending in this application.

§112 Rejection of the Claims

Claims 1-23 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The Office indicated that the limitation "creating" in claims 15-23 was lacking antecedent basis. Applicant has amended claims 15 and 21 to change "creating" to "adding" to provide proper antecedent basis.

Also, the Office indicated that "[i]t is unclear how anything is either added or created." Office Action at ¶2. Applicant respectfully traverses the rejection. The bypass logic is added by adding the elements that are coupled together as noted in the subsequent limitations of the claims. For example, the bypass logic is added by coupling a first latency delay unit to the conditional state element. Also, see the description of Figures 1A-1E for discussion of the elements being added as such elements are coupled together during the transforming. Accordingly, Applicant respectfully submits that claims 1-23 are sufficiently definite and that the rejection of such claims under 35 USC § 112, second paragraph, has been overcome.

§102 Rejection of the Claims

Claims 1-3, 5, 8-11, 15-17, and 21 were rejected under 35 USC § 102(b) as being anticipated by Vashi (U.S. 6,219,819). Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration.[1] Applicant respectfully traverses the rejection.

Among the differences, claim 1 recites "adding a bypass logic into a digital circuit design, wherein the adding comprises transforming a conditional state element into a logically redundant element in the digital circuit design." The Office indicated that this limitation is

[1] *In re Dillon* 919 F.2d 688, 16 USPQ2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991).

disclosed by Vashi at Figure 3 and column 4.[2] Vashi generally relates to allowing "a design implemented in a configurable FPGA to be implemented in a non configurable (HardWire) device without problems due to changes in timing."[3] Vashi at column 4 relates to a computer system used for performing the operations for changing from a configurable FPGA to a non configurable device. Figure 3 of Vashi relates to a design that includes "paths dedicated to testing" that "should be bypassed during timing analysis of the HardWire device."[4] Figure 3 illustrates multiplexers and flip-flops coupled together. However, Vashi does not disclose a transforming of a conditional state element into a logically redundant element.

Claims 8, 15 and 21 disclose similar limitations. Accordingly, because the cited reference does not disclose all of the claim limitations, Applicants respectfully submit that the rejection of claims 1, 8, 15 and 21 under 35 U.S.C. §102 has been overcome. Claims 2-3, 5; claims 9-11 and claims 16-17 depend from, respectively, claims 1, 8 and 15 and distinguish the reference for at least the same reason.

§103 Rejection of the Claims

Claims 22-23 were rejected under 35 USC § 103(a) as being unpatentable over Vashi (U.S. 6,219,819) in view of McFarland (U.S. 6,212,629). Because claims 22-23 depend from and further define claim 21, Applicant respectfully submits that the rejection of claims 22-23 under 35 U.S.C. §103 has been overcome.

Allowable Subject Matter

Claims 4, 6-7, 12-14, and 18-20 were indicated to be allowable if rewritten to overcome the rejection(s) under 35 USC § 112 set forth in the Office Action. Applicant acknowledges the allowable subject matter.

The Office Action indicated reasons for allowable subject matter. The Office Action uses the term "prior art." However, Applicant does not make any admissions regarding the prior-art status of any references in the record of the application. Instead, Applicant regards these references as only being "of record." Additionally, Applicant submits that the Office Action

[2] Office Action at page 6.
[3] Vashi at column 2, lines 57-60.
[4] Vashi at column 6, lines 1-7.

makes numerous assertions regarding the interpretations of limitations of the claims, the contents of the art and distinguishing features of the claims. Applicant has neither verified nor accepted the accuracy of these assertions, and respectfully submits that there may be different interpretations that those identified in the Office Action. Additionally, Applicant respectfully submits that the relevant claims may be allowable for one or more reasons in addition to and/or in alternative to those reasons identified in the Office Action. Applicant reserves the right to further address one or more aspects of the reasons for allowance as may later be necessary or desirable.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 371-2103) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 1st day of December 2006.

Amy Moriarty
Name

Signature